

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

PREDICTION OF WIRELESS COMMUNICATION SYSTEMS PERFORMANCE IN INDOOR APPLICATIONS

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Master of Science in Electrical Engineering-December 2000

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Due to a shift in the interest in wireless applications, from outdoor to indoor environments, new modelling solutions had to be designed to account for the immense complexity of the latter. Essentially, two categories of indoor propagation models prevailed until the mid-90s: the empirical and the physical models. They both predicted important characteristics of a given confined environment like the coverage area, transmitted power requirements, number and location of base stations or access points. The implementation of wireless communications systems onboard naval assets is expected to offer numerous advantages and enhance the existing shipboard communications systems. That, in turn, calls for a reliable and cost-effective means of estimating the expected link budget in such environments, especially when the infrastructure in question is yet to be built, as is the case in a ship class under development.

This thesis treats the problem of indoor propagation modeling using the Numerical Electromagnetic Code-Basic Scattering Code (NEC-BSC) and compares the predicted results obtained by this code with actual measurements performed inside a building at the Naval Postgraduate School. A number of important conclusions regarding the validity of NEC-BSC for indoor applications are being reached and some intriguing statistical results are being presented.

DoD KEY TECHNOLOGY AREA: Command, Control, and Communications

KEYWORDS: Simulation of Signal Propagation, Indoor Radio Propagation, NEC-BSC

DESIGN OF A SYNCHRONOUS PIPELINED MULTIPLIER AND ANALYSIS OF CLOCK SKEW IN HIGH-SPEED DIGITAL SYSTEMS

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Digital systems implemented with high-speed transistor technologies face a variety of design challenges in an effort to keep pace with the accelerating demand for performance. As device switching frequencies climb comfortably into the gigahertz range, clock skew in digital systems threatens to limit the advantages of synchronous pipelined designs. This research investigates the limitations of clock skew on high-speed digital systems by designing and simulating an 8x8 bit synchronous, pipelined multiplier using Indium phosphide (InP), heterostructure bipolar junction (HBT) transistor technology. Fundamentals of circuit analysis and the principles of junction transistor behavior are applied to design an optimal family of logic devices using current-mode logic. All testing and simulation data is based upon results obtained from Tanner SPICE design tools. Using the building blocks of this logic family, an array multiplier is

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constructed and further configured into five distinct pipeline implementations. By employing a different number of pipeline stages in each implementation, the trade-offs of pipelining are illustrated and clock skew is analyzed at a variety of throughput rates. Finally, the impact of clock skew on throughput performance is quantified and summarized as a reference point for further research into asynchronous control techniques.

DoD KEY TECHNOLOGY AREA: Electronics

KEYWORDS: Clock Skew, Pipelined Logic Architecture, Current-Mode Logic, Indium-Phosphide Heterojunction Bipolar Transistors, High-Speed Logic

AN INVARIANT DISPLAY STRATEGY FOR HYPERSPECTRAL IMAGERY

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Remotely sensed data produced by hyperspectral imagers contains hundreds of contiguous narrow spectral bands at each spatial pixel. The substantial dimensionality and unique character of hyperspectral imagery requires display techniques that differ from traditional image analysis tools.

This study investigated the appropriate methodologies for displaying hyperspectral images based on the physical principles of human color vision and a generalized set of linear transformations. Principal components (PC) analysis is a powerful tool for reducing the dimensionality of a data set, and PC-based strategies were explored in creating a broadly applicable image display strategy. It is shown that the invariant display strategy and generalized eigenvectors developed within this study offer a first look capability for a wide variety of spectral scenes. PC transformations utilizing this generalized set of eigenvectors allow for 'real time' initial classification. Detailed investigation of the relationship between the PC eigenvectors and dissimilar image content shows that this strategy is robust enough to provide an accurate initial scene classification.

DoD KEY TECHNOLOGY AREAS: Sensors, Human Systems Interface

KEYWORDS: Spectral Imagery, Display Strategies, Colorimetric Representations, Hyperspectral Analysis

WEARABLE HF ANTENNA FOR NAVAL POSTGRADUATE SCHOOL COMWIN SYSTEM

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Researchers at the Naval Postgraduate School (NPS) have proposed a Combat Wear Integration (COMWIN) antenna system that includes three separate antennas for the man-portable implementation of the Joint Tactical Radio System (JTRS). The COMWIN system incorporates wideband antennas into the warrior's combat clothing in order to make the radio operator indistinguishable on the battlefield. The three antennas cover the frequency ranges: 2-30 MHz, 30-500 MHz, and 500-2000 MHz. This thesis describes the man wearable HF antenna designed to operate from 2-30 MHz for use by dismounted warriors in all combat environments. The antenna was designed and its performance predicted using Ansoft's High Frequency Structure Simulator (HFSS) and Nittany Scientific, Inc.'s Graphical Numerical Electromagnetics Code (GNEC). Measurements of the prototype showed good agreement with theoretical

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predictions. The HF antenna must operate with an inductive Automatic Tuning Unit (ATU). Coupling between the antenna and a human body effects antenna input impedance. Placing the antenna on a human limits the antenna conductor electrical path length at the frequencies of operation. For the optimum antenna location, an analysis of the antenna design is conducted for seven different types of soil. The antenna must operate from 2-30 MHz with a Voltage Standing Wave Ratio (VSWR) less than three for a 50 Ω coaxial cable, have low visual signature, be vertically polarized, have coverage from 0 to 60 degrees above the horizon and 0 to 360 degrees in azimuth. Input impedance and radiation patterns are determined for the antenna using the GNEC and HFSS.

DoD KEY TECHNOLOGY AREAS: Battle Space Environments, Clothing, Textiles and Food, Command, Control and Communications, Electronics, Electronic Warfare, Modeling and Simulation, Manufacturing Science and Technology

KEYWORDS: HF Antenna, Wearable Antenna, Numerical Electromagnetics Code (NEC), Method of Moments, Combat Wear Integration

PERFORMANCE ASSESSMENT OF AN INTRAPULSE TECHNIQUE TO IDENTIFY AND DEINTERLEAVE RADAR SIGNALS

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The Wilson Advanced Specific Emitter Identification (SEI) Algorithm with Adaptive Thresholds is evaluated using live radar data. The objective is to determine performance of the algorithm in a low signal to noise ratio (SNR) environment, compare the performance to that of an intrapulse frequency based approach and explore implementation of the algorithm in deinterleaving applications. Utilizing unintentional Phase Modulation on the Pulse (PMOP) as an identification feature and adaptive thresholds in the classifier, the algorithm is designed to identify radar signals based on single pulse analysis. Earlier efforts have demonstrated the efficacy of using PMOP versus frequency modulation on the pulse (FMOP) and the technique's effectiveness against lab generated signals in low SNR conditions. This work tests the technique utilizing live radar data. Live radar data of marine navigation radars with similar conventional parameters collected by the Naval Research Laboratory served as the data set for the test. The SEI results of the live radar testing confirm the algorithm performs well on a single pulse basis in relatively low SNR environments. Additionally, use of PMOP in the algorithm results in a 3-4 dB SNR performance gain over FMOP. A conceptual deinterleaving architecture, which incorporates the technique, is developed.

DoD KEY TECHNOLOGY AREAS: Battlespace Environments, Command, Control, and Communication, Electronics, Electronic Warfare, Sensors, Space Vehicles

KEYWORDS: Specific Emitter Identification, Deinterleaving, Intrapulse, Unintentional Modulation on the Pulse, Pattern Recognition, Signal Classification, SNR

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DESIGN AND EXPERIMENTAL EVALUATION OF AN ELECTRO-OPTICAL, SIGMA-DELTA MODULATOR FOR WIDEBAND DIGITAL ANTENNAS

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Electro-optical sigma-delta ($\Sigma\Delta$) analog-to-digital converters (ADCs) use a pulsed laser to oversample an input signal at two Mach-Zehnder interferometer modulators. A fiber lattice accumulator is embedded within a feedback loop around a single-bit quantizer to spectrally shape the quantization noise to fall outside the signal band of interest. Applications of electro-optical $\Sigma\Delta$ ADCs include digitizing wideband radio frequency signals directly at an antenna (digital antenna). The design considerations, construction process and experimental evaluation of the electro-optical $\Sigma\Delta$ ADC are presented. The experimental results are compared with a computer model of the electro-optical $\Sigma\Delta$ sampling and digitization process.

DoD KEY TECHNOLOGY AREAS: Electronics, Electronics Warfare, Sensors, Other (Electro-Optics)

KEYWORDS: Sigma-Delta, Optical Sampling, Analog-to-Digital Converters, Optical ADC, Electro-Optical, Digital Antennas, Fiber Lattice, Mach-Zehnder Interferometers

EFFECTIVENESS OF THE HARM AS EMPLOYED BY THE F-16CJ AIRCRAFT AGAINST SERBIAN THREAT AND EARLY WARNING RADAR DURING OPERATION ALLIED FORCE

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The purpose of this thesis is to quantify the effectiveness of HARM Employment by F-16CJ aircraft against Serbian Threat and EW radars during OPERATION ALLIED FORCE (OAF) of March-June 99. The effectiveness was determined primarily through the use of "all-source" data to confirm the suppression/damage that target radars may have suffered and to assess general radar activity impacts as a whole during the conflict. The factors that enhance or degrade HARM effectiveness were also investigated as well as strike aircraft impacts where possible. Due to the impact that fog of war has on obtaining specific technical data, the emphasis of the report is on the apparent effect of the HARM on the enemy air defenses during the course of a mission (and campaign) and not the technical aspects of HARM performance during an engagement. However, modeling of several of the individual mission incidents was accomplished. In these cases, MESA 5.1.3 (Model for Electronic Support and Attack) was used to model the airborne receivers/ground emitters, calculate propagation losses, and verify scenario geometry to determine signal strength levels at the airborne receivers of interest.

DoD KEY TECHNOLOGY AREA: Electronic Warfare

KEYWORDS: F-16CG, High-Speed Anti-Radiation Missile, Air War Over Serbia

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COMPLETION AND TESTING OF A TMR COMPUTING TESTBED AND RECOMMENDATION FOR A FLIGHT-READY FOLLOW-ON DESIGN

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This thesis focuses on the completion and hardware testing of a fault tolerant computer system utilizing Triple Modular Redundancy (TMR). Due to the radiation environment in space, electronics in space applications must be designed to accommodate single event phenomena. While radiation hardened processors are available, they offer lower performance and higher cost than commercial off the shelf processors. In order to utilize non-hardened devices, a fault tolerance scheme such as TMR may be implemented to increase reliability in a radiation environment. The design that was completed in this effort is one such implementation.

The completion of the hardware design consisted of programming logic devices, implementing hardware design corrections, and the design of an overall system controller. The testing effort included basic power and ground verification checks to programming, executing, and evaluating programs in read only memory. During this phase, additional design changes were implemented to correct design flaws.

This thesis also evaluated the preliminary design changes required for a space implementation of this TMR design. This included design changes due to size, power, and weight restrictions. Additionally, a detailed analysis of component survivability was performed based on past radiation testing.

DoD KEY TECHNOLOGY AREAS: Space Vehicles, Computing and Software, Electronics

KEYWORDS: Fault Tolerant Computing, Triple Modular Redundancy (TMR), Commercial-off-the-Shelf (COTS) Devices, Single Event Upsets (SEU)

ANALYSIS OF MULTIRATE RANDOM SIGNALS

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Multirate digital signal processing techniques have been developed in recent years for a wide range of applications, such as speech and image compression, digital audio, statistical and adaptive signal processing, numerical solution of differential equations and many other fields.

The purpose of this thesis is to extend optimal filtering techniques to random signals sampled at different rates. In particular, two major problems are considered: (1) optimal filtering of two sets of observations at different sampling rates as a multirate Wiener filter, and (2) linear prediction on successive samples of a random process. In the first problem it is shown that the standard Wiener filter can be extended to the multirate case, while preserving its optimality. In the second problem it is shown that multichannel linear prediction on successive samples of a process, yields orthogonal uncorrelated innovations.

DoD KEY TECHNOLOGY AREAS: Electronics, Computing and Software, Sensors

KEYWORDS: Multirate Signal Analysis, Estimation, Wiener Filter

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THE DESIGN, SIMULATION, AND FABRICATION OF A VLSI DIGITALLY PROGRAMMABLE GIC FILTER

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In this research, the design, simulation and mask layout for a VLSI Digitally Programmable Generalize Impedance Converter (GIC) Filter is presented. Programmable elements are filter type (low-pass, high-pass, band-pass and notch), center frequency and quality factor. The analog design eliminates the quantization errors, analog-to-digital and digital-to-analog conversion components, and the processing time delay associated with digital signal processing devices. Using a GIC as the basic circuit simplifies topology changes to realize the programmability function and eliminates a problematic component for integrated circuit fabrication, the inductor. Additionally, switched capacitor usage allows the elimination of resistors from the design, another problematic component for integrated circuits. The design was simulated with PSPICE while VLSI mask layout was performed with LASI. The chip has been submitted for fabrication to further research the design of analog VLSI circuits.

DoD KEY TECHNOLOGY AREA: Electronics

KEYWORDS: GIC, Analog Filter, VLSI, Switched Capacitor, Programmable Filter

DESIGN AND PERFORMANCE ANALYSIS OF AN ASYNCHRONOUS PIPELINED MULTIPLIER WITH COMPARISON TO SYNCHRONOUS IMPLEMENTATION

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Synchronous techniques have dominated digital logic system design for decades because they are well understood and less complicated to implement. With the advent of more exotic high-speed transistors, the issues of clock skew, system performance, power consumption, and technology migration become critical to synchronous system designers. Asynchronous digital design techniques utilize a local completion signal or request/acknowledge handshake to lend the stability afforded by the global clock in synchronous systems. This research evaluates a moderately complex digital system, an 8x8-bit multiplier utilizing high speed Indium Phosphide heterostructure bipolar junction transistors, to determine whether asynchronous logic design can compete with synchronous design in terms of system speed and power consumption. Theoretical timing equations are developed that relate the relative merits of each technique for input-to-output latency and system throughput. Tanner SPICE simulation tools are used to evaluate the full 8x8-bit asynchronous array multiplier. Finally, direct comparisons are made between five separate pipelined configurations of the multiplier utilizing both synchronous and asynchronous timing methodologies. As integrated circuits become smaller, faster, and more complex, asynchronous schemes will continue to mature and become more prevalent in digital system design.

DoD KEY TECHNOLOGY AREA: Electronics

KEYWORDS: Asynchronous Logic, Pipelined Logic, Micropipelines

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SIMULATION AND PERFORMANCE ANALYSIS OF THE AD HOC ON-DEMAND DISTANCE VECTOR ROUTING PROTOCOL FOR TACTICAL MOBILE AD HOC NETWORKS

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This thesis presents a simulation and analysis of the Ad Hoc On-Demand Distance Vector Routing Protocol (AODV) for mobile ad hoc network (MANET) environments using the Network Simulator 2 (NS2) tool. AODV is being suggested for possible implementation in the Joint Tactical Radio System (JTRS) for the United States military. Utilizing an AODV model resident in NS2, the simulation focuses on key performance parameters that include the packet delivery fraction, routing loss, buffer loss, total loss, throughput and goodput. The AODV node movement and traffic connection files have been generated to measure the network performance for a given environment using specific parameters. The results reported in this thesis indicate that the network environment size, packet rate and offered load are critical to the network performance. Node velocity played a minimal role in affecting the overall network performance.

DoD KEY TECHNOLOGY AREAS: Command, Control, and Communication, Computing and Software, Modeling and Simulation

KEYWORDS: Joint Tactical Radio System, Mobile Ad Hoc Network, Network Simulator 2, Protocol Analysis, Ad Hoc On-Demand Distance Vector Routing

