

# MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

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## **THERMINATOR: CONFIGURING THE UNDERLYING STATISTICAL MECHANICS MODEL**

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The rapid increase in sophisticated Internet attacks has left the security industry lagging far behind. In an attempt to improve network security, Therminator, a patternless intrusion detection system, was developed in 2001 by NPS in conjunction with NSA. The Therminator model uses statistical mechanics to analyze network traffic as a system of exchanges. Being highly configurable enables Therminator to be adapted for any network configuration. Until now, however, no exploration had been conducted on the configuration parameters of the underlying statistical mechanics model. It is important to understand the effects of these parameters to optimize anomaly detection. Thus, the current study explored these parameters using HTTP traffic generated in a controlled test environment. Results were as follows: equations were developed for state counting to determine bucket state space sizes; bucket state space size was found to be symmetrical about the midpoint of the boundary conditions; proper display period was based on traffic rate; and lastly, the more orthogonal anomalous traffic was to the normal traffic, the larger the perturbation was in the state graph. These results provide needed insight into properly configuring Therminator for optimal anomaly detection, ultimately affording the Department of Defense greater network security.

**KEYWORDS:** Network Security, Network Assurance, Information Protection, Intrusion Detection, Patternless Intrusion Detection, Network Anomaly Detection, Real-Time Network Monitoring, Statistical Mechanics

## **TESTING AND EVALUATION OF THE CONFIGURABLE FAULT TOLERANT PROCESSOR (CFTP) FOR SPACE-BASED APPLICATIONS**

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With the complexity of digital systems, reliability considerations are important. In many digital systems, it is desirable to continuously monitor, exercise, and test the system in order to determine whether the system is performing as desired. Such monitoring may enable automatic detection of failures via periodic testing or through the use of codes and checking circuits (e.g., built-in self-testing). While any complex system requires testing to ensure satisfactory performance, satellite systems require extensive testing for two additional reasons: they operate in an environment considerably different from that in which they were built, and after launch they are inaccessible to routine maintenance and repair. Because of these unique requirements, a specific solution is required, such as a self-contained, autonomous, self-testing circuit. The focus of this thesis is on the design and development of a series of Built-In Self-Tests (BISTs) for use with the Configurable Fault Tolerant Processor (CFTP). The results of this thesis are two detailed designs for a Random Access Memory (RAM) BIST and a Read-Only Memory (ROM) BIST, as well as a conceptual design for a Field Programmable Gate Array (FPGA) BIST. These designs are stored on board the CFTP and are made to operate remotely and autonomously. Together, these BISTs provide a means to monitor, exercise, and test the CFTP components and thus facilitate a reliable design.

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**KEYWORDS:** Field-Programmable Gate Array, FPGA, Built-In Self-Test, BIST, FPGA Testing, Read-Only Memory Testing, ROM Testing, Random Access Memory Testing, RAM Testing, System Diagnosis, System Reliability

## EFFECTS OF RADIOWAVE PROPAGATION IN URBANIZED AREAS ON UNMANNED AERIAL VEHICLE-GROUND CONTROL STATION COMMAND AND CONTROL

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The purpose of this research was to examine the effects of radiowave propagation in urbanized areas on unmanned aerial vehicle-ground control station (UAV-GCS) command and control.

Operating at high frequency has merits of higher data rate transfer, which is crucial to support the large quantity of voice and video data to be transmitted via UAV-GCS linkage. However, high frequencies are attenuated more rapidly in glossy materials and weather. Having a shorter operational range translates to a smaller RF spread radius, and thus lowers the susceptibility to detection and jamming.

The software, Urbana, was used to investigate the propagation of radio signals in urban environments under varying conditions. Simulations were conducted for a small group of buildings and a large collection of buildings representative of a big city. The data clearly illustrate the effect of “urban canyons” and diffraction around buildings.

An UAV deployed for military operations in urban terrain (MOUT) must have the inherent capability to hover or fly at low speeds to be able to adapt to the dynamic urban environment and to capitalize on communications opportunities. Simulations show that a single UAV hovering at three times the height of the tallest building in the central city was found to provide concentric, uniform signal coverage.

**KEYWORDS:** Unmanned Aerial Vehicles, Urbana Wireless Toolset, Propagation Models, Airborne Communications Node, Portable Ground Control System

## BENCHMARKING AND ANALYSIS OF THE SRC-6E RECONFIGURABLE COMPUTING SYSTEM

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This thesis evaluates the usefulness of the SRC-6E reconfigurable computing system for a radar signal processing application and documents the process of creating and importing VHDL code to configure the user definable logic on the SRC-6E. A false target radar imaging algorithm is chosen and implemented on the SRC-6E. Data from alternative computational approaches to the same problem are compared to determine the effectiveness of the SRC-6E solution. The results show that the implementation of the algorithm does not provide an effective solution when executed on the SRC-6E. An evaluation of the SRC-6E difficulty of use is conducted, including a discussion of required skills, experience, and development times. The algorithm test code and collected data are included as appendices.

**KEYWORDS:** Benchmark, Reconfigurable Computing, VHDL, SRC-6E, FPGA, False Radar Target Synthesis

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## RECURSIVE PARAMETER IDENTIFICATION FOR ESTIMATING AND DISPLAYING MANEUVERING VESSEL PATH

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Real-time recursive parameter identification is applied to surface vessel modeling for maneuvering path prediction. An end-to-end system is developed to simulate vessel motion, identify vessel parameters, and estimate future path. Path prediction improves bridge team situational awareness by providing a real-time depiction of future motion over the ground on an electronic chart and display system (ECDIS). The extended least-squares (ELS) parameter identification approach allows the system to be installed on most platforms without prior knowledge of system dynamics, provided vessel states are available. The system continually tunes to actual environmental conditions, including vessel ballasting, current, wind, and sensor biases. In addition to path prediction, the system estimates maximum vessel roll angle during maneuvering. Maximum roll prediction enhances carrier flight deck safety and increases operational effectiveness by reducing sea room requirements. Suitable performance is demonstrated in real world maneuvering conditions to recommend that maneuvering path prediction be incorporated into the U.S. Navy's AN/SSN-6 Navigation Sensor System Interface (NAVSSI) electronic charting system. Future research should emphasize an underway demonstration with real-time data acquisition.

**KEYWORDS:** Recursive Parameter Estimation, Electronic Chart and Display System, ECDIS, ECN, AN/SSN-6, NAVSSI, Vessel Dynamic Model, Path Prediction

## TRIPLE MODULAR REDUNDANCY (TMR) IN A CONFIGURABLE FAULT-TOLERANT PROCESSOR (CFTP) FOR SPACE APPLICATIONS

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Without the protection of atmosphere, space systems have to mitigate radiation effects. Several different technologies are used to deal with different radiation effects in order to keep the space device working properly. One of the radiation effects, called Single Event Upset (SEU), can change the state of a component or data on the bus. A single error could possibly cause a system failure if it is not corrected.

Besides error correction, a space system also needs the flexibility to be modified or upgraded easily. Consequently, the idea of having a TMR design instantiated in an FPGA to construct a Configurable Fault-Tolerant Processor (CFTP) developed. The TMR, which runs one program in three identical soft-core processors with voters, is a scheme used to mitigate an SEU. The full design of TMR running in an FPGA functions as a System-On-a-Chip (SOC). Both soft-core processor and FPGA offer the CFTP a great flexibility to be reconfigured.

A complete TMR design includes some fundamental components besides processors and voters, such as the *Reconciler*, *Interrupt* and *Error Syndrome Storage Device (ESSD)*. These components have their unique function in the TMR design. They are created and simulated. It is important to always keep in mind factors that affect test bench settings, such as processor pipelining. A component is designed to implement proper functions first. Then it is revised to work with the processor and memory. The full design for the TMR in this thesis proves its ability to detect and correct an SEU. The follow-on research suggested is to improve the efficiency and performance of this design.

**KEYWORDS:** Single Event Upset, SEU, Configurable Fault-Tolerant Processor, CFTP, TMR, FPGA, System-On-a-Chip, SOC, Reconciler, Interrupt and Error Syndrome Storage Device, ESSD