

MODELING SINGLE-EVENT TRANSIENTS IN COMPLEX DIGITAL SYSTEMS

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A methodology to determine the effect of single-event transients (SETs) on complex digital systems has been developed. This methodology is based on the SET state-transition model. This model breaks the complex digital system down into five states. These states are the error-free/transient-free state, the logic-gate transient state, the single-event-upset (SEU) state, the output-driver transient state, and the failure state. The state-transitional probabilities of the model are determined by SET generation modeling, SET propagation modeling, and SEU propagation modeling. SET generation and propagation are primarily modeled using SPICE. SEU propagation modeling is accomplished using a combination of VHDL fault-injection modeling and mode-dependent (or instruction-based for a processor) register-usage analysis.

To verify this methodology, the SET tolerance of a 16-bit RISC microprocessor, the KDLX, was predicted. The transitional probabilities for this processor were determined, and the effective cross-section of the processor for three different test programs was predicted. Laser testing was performed on the KDLX to validate the predicted transitional probabilities. Heavy-ion testing was performed to validate system-level predictions. The results from the heavy-ion testing show that the methodology accurately predicts the saturated effective cross-section of a complex digital system.

KEYWORDS: Single-Event-Transients, Single-Event-Upsets, Single-Event-Effects, Transient Fault Propagation